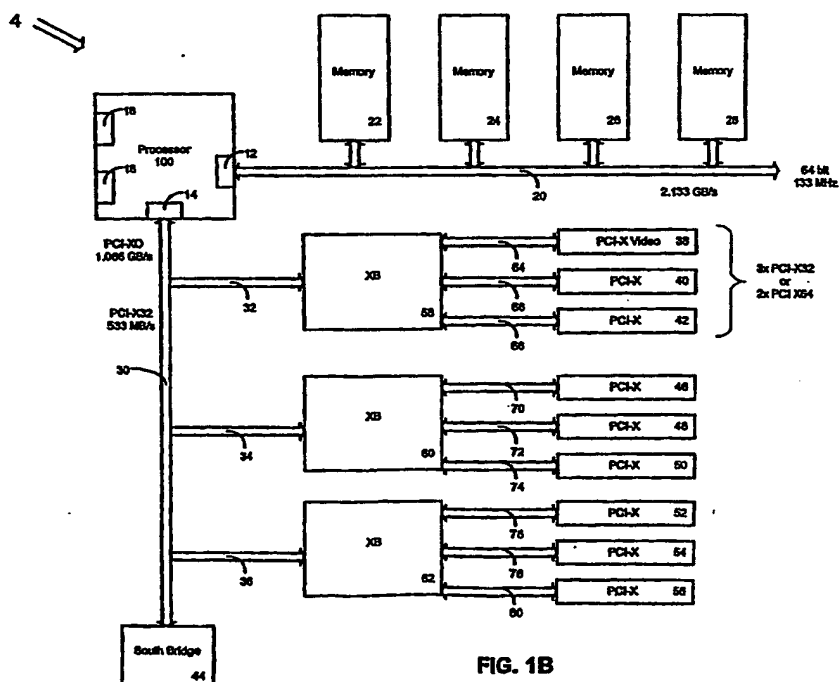


**FIG. 1A**



**FIG. 1B**

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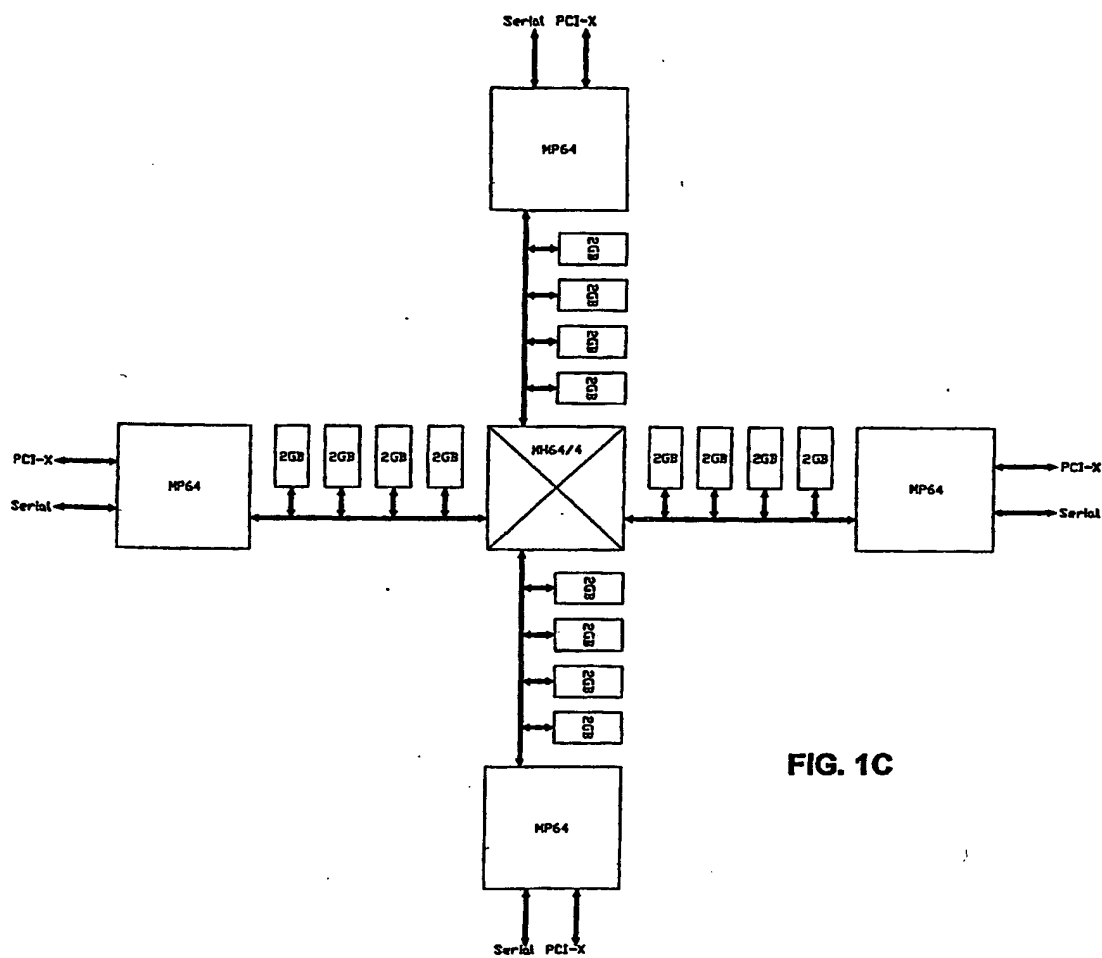
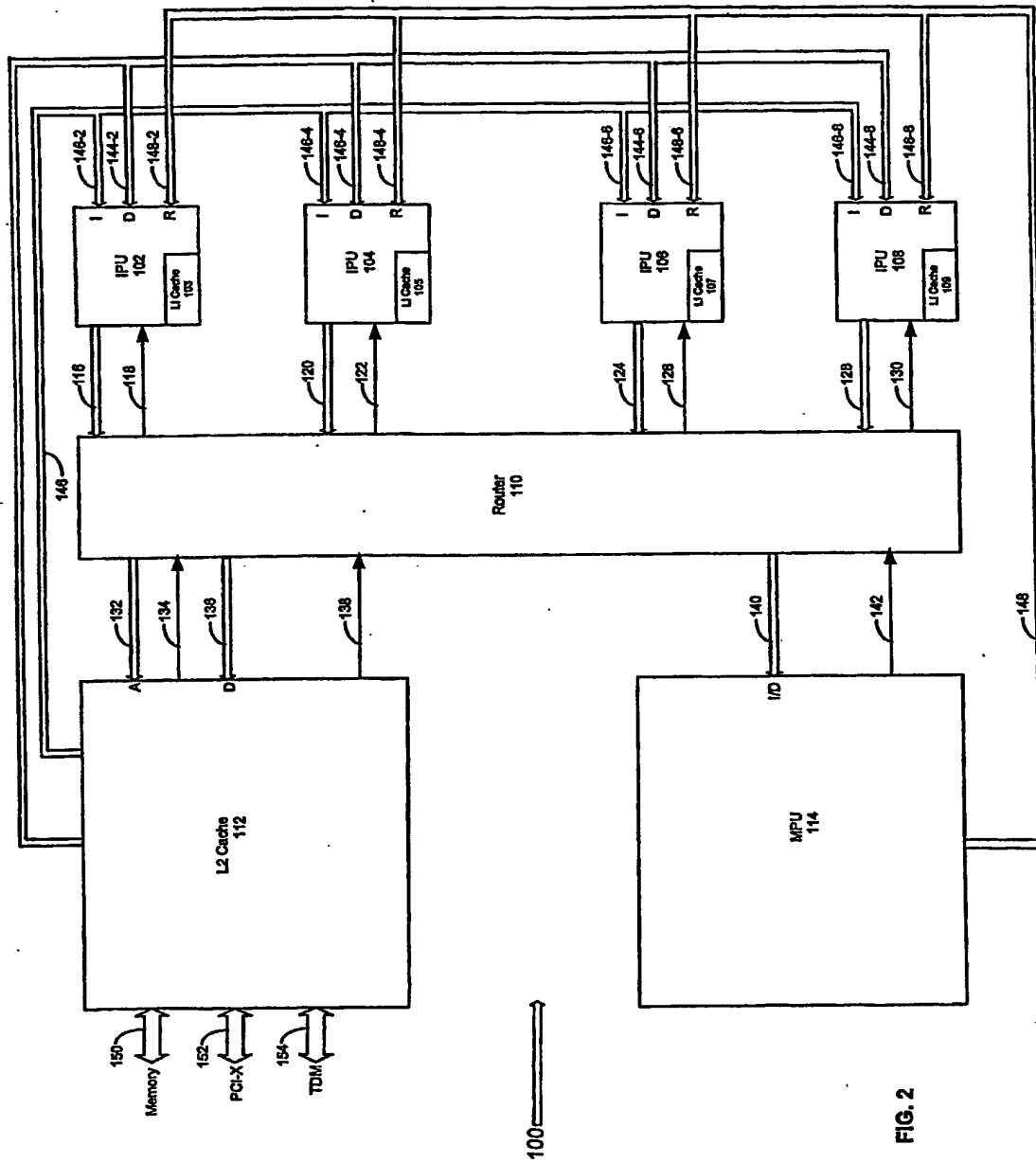


FIG. 1C



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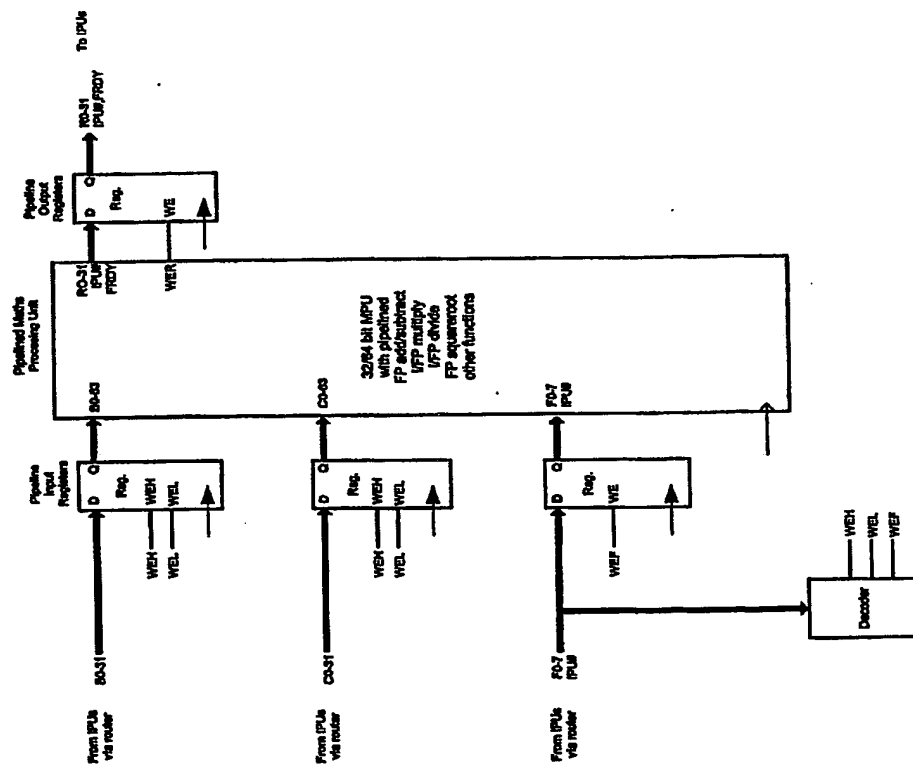


FIG. 3

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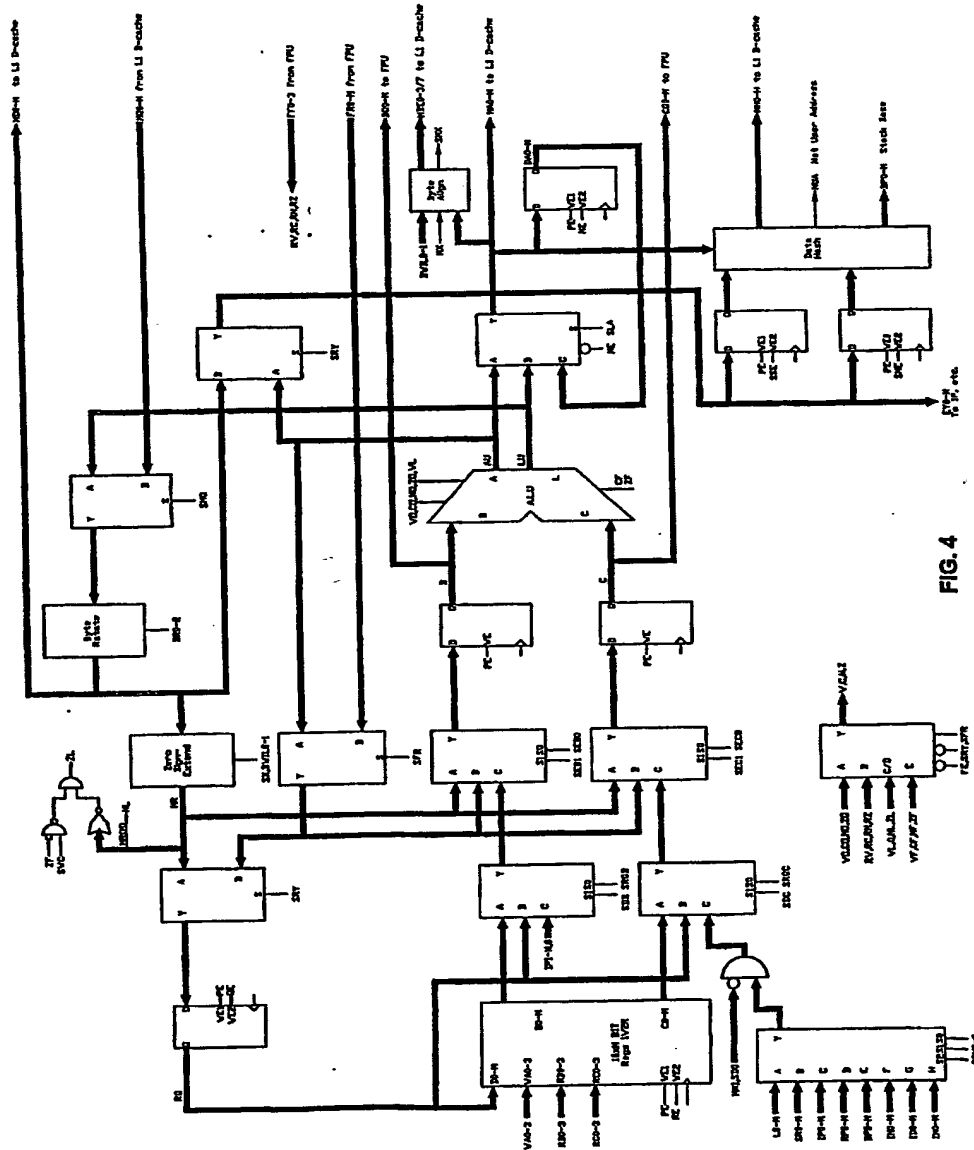


FIG. 4

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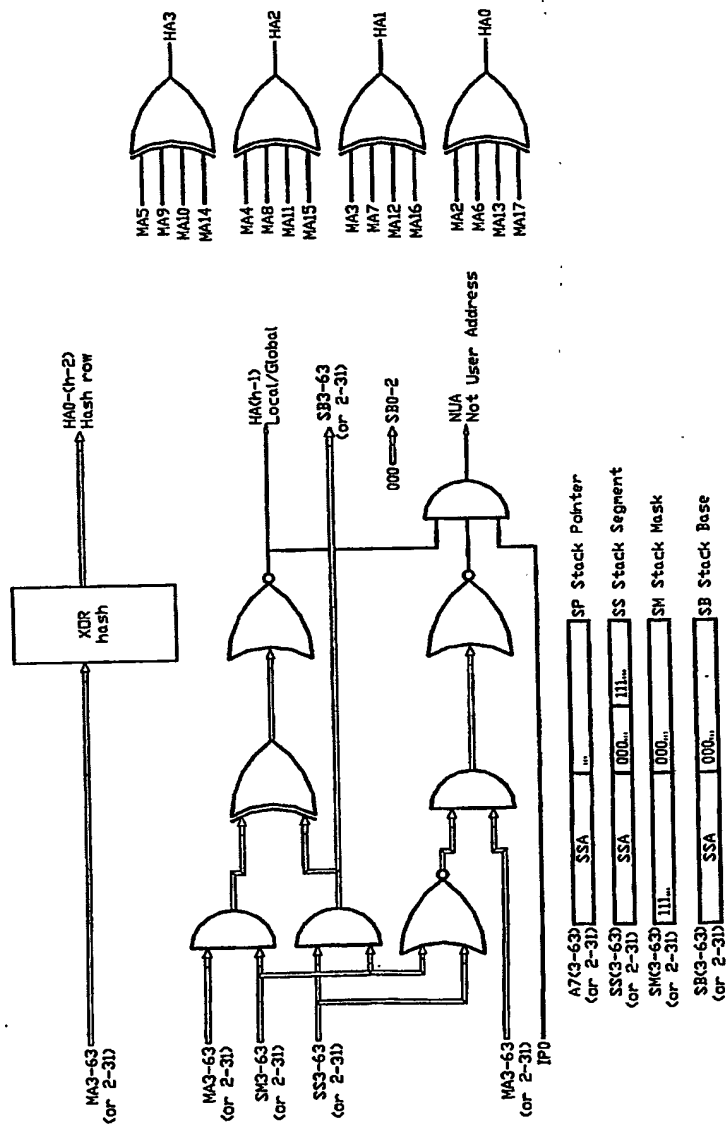
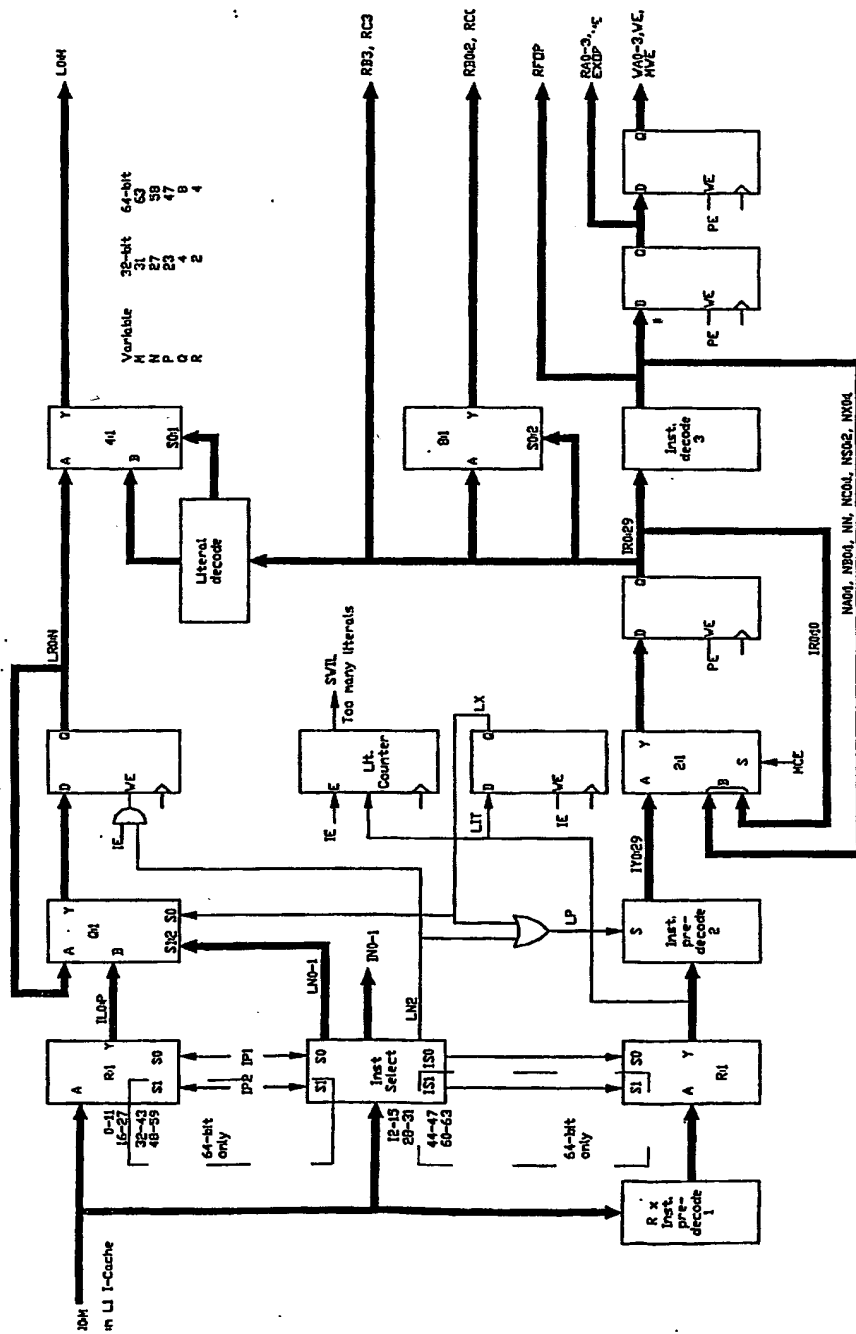
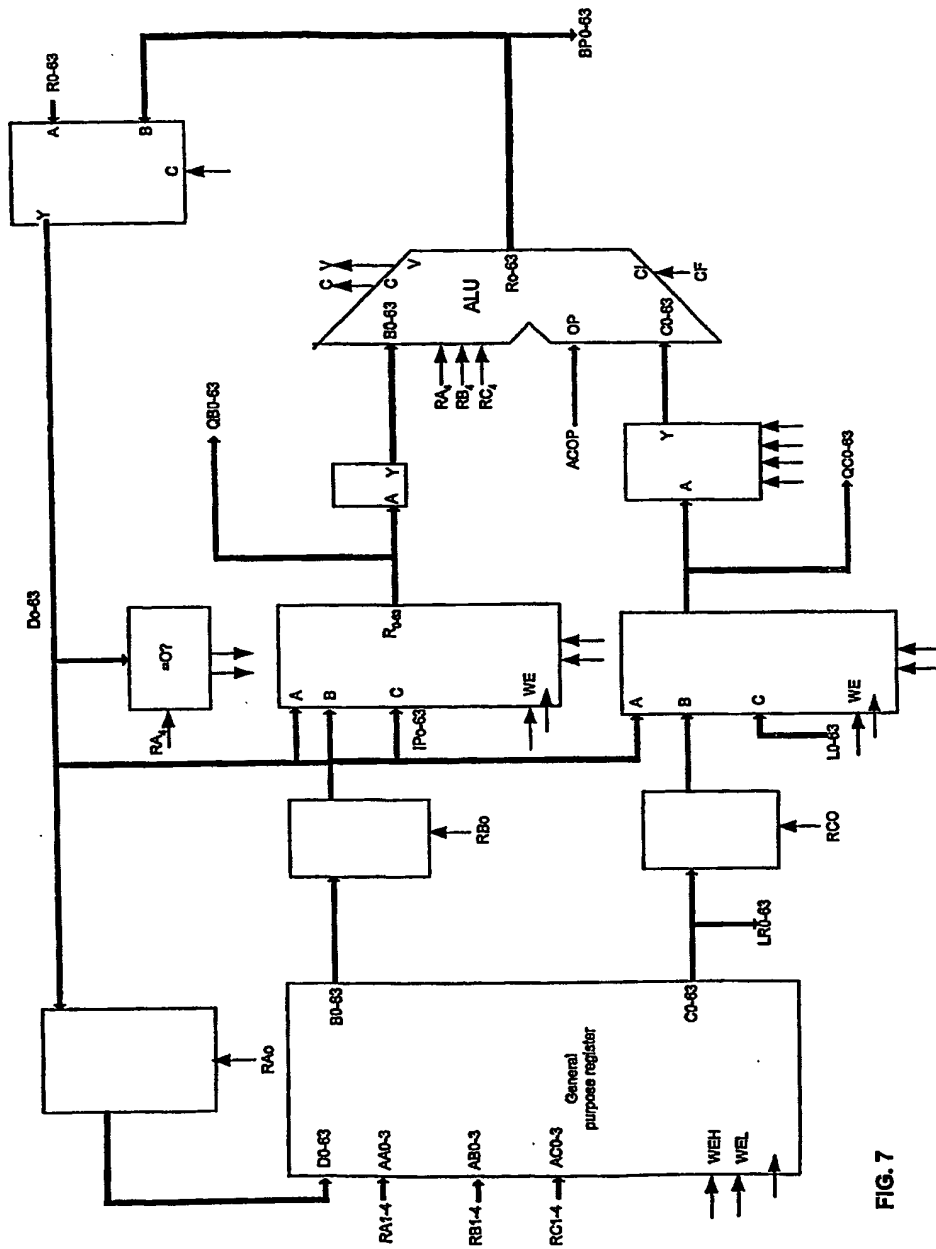


FIG. 5

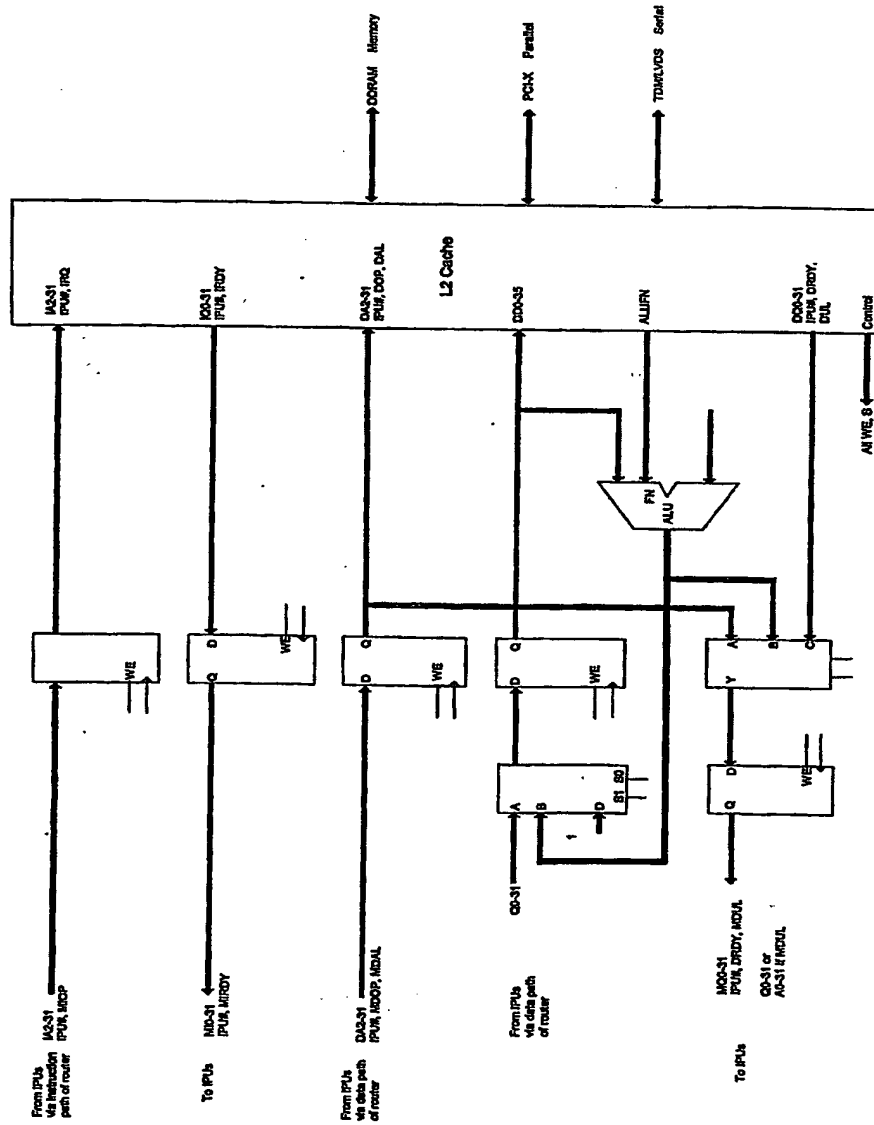


**FIG. 6**



**FIG. 7**





**FIG. 8**

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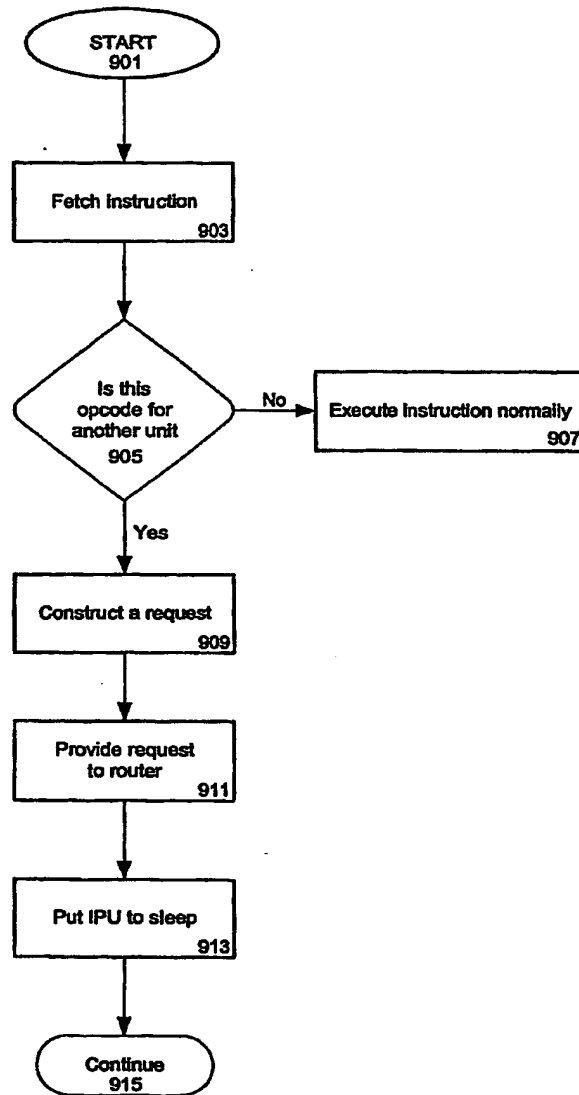


FIG. 9

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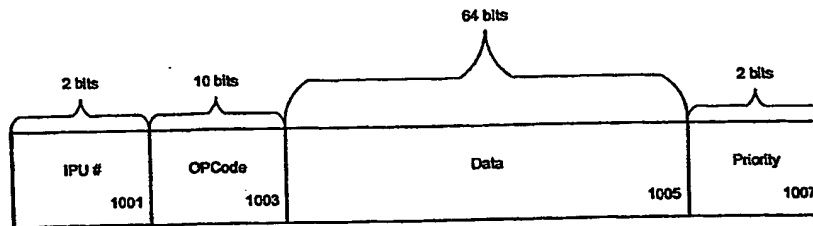


FIG. 10

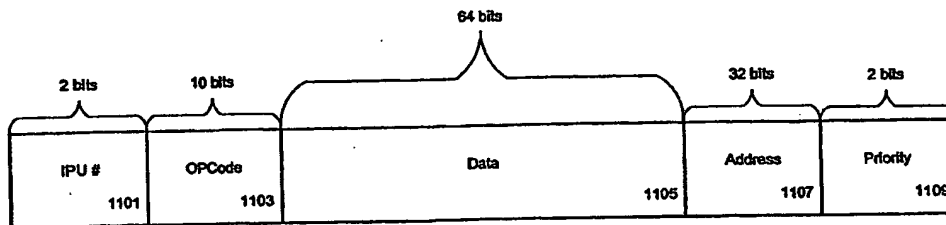


FIG. 11

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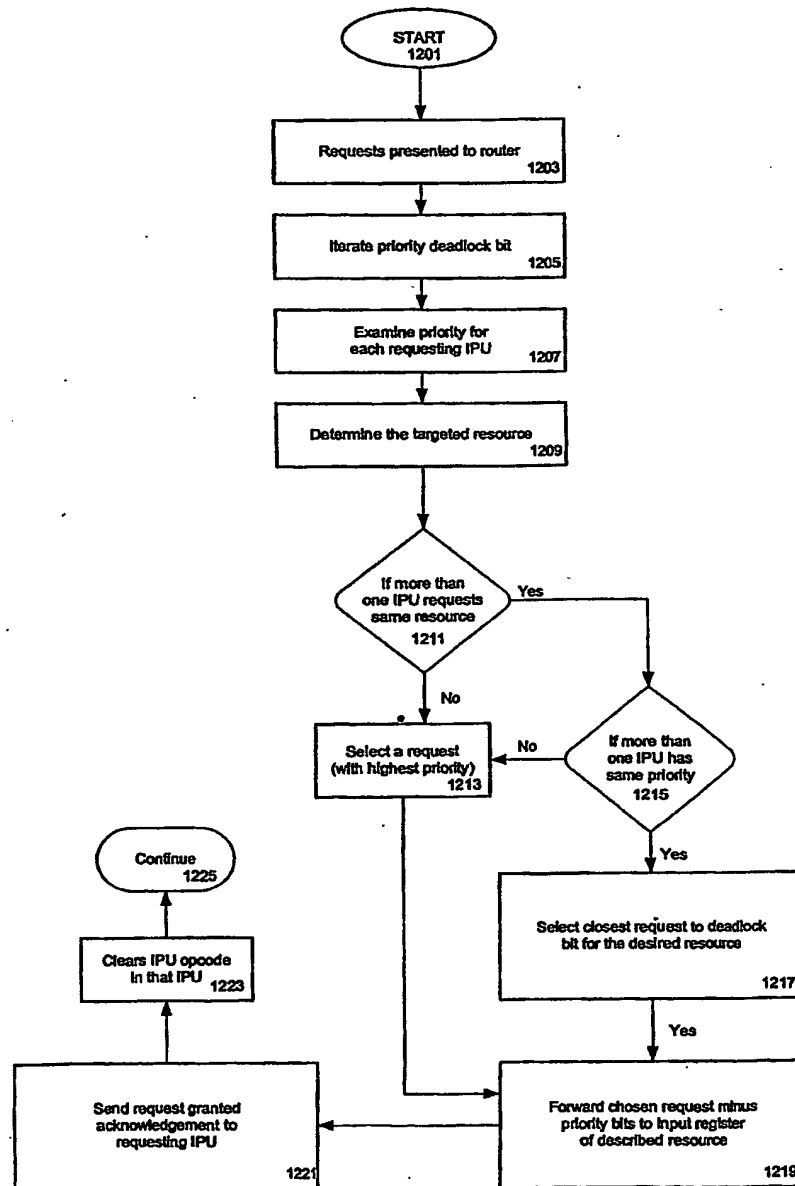


FIG. 12

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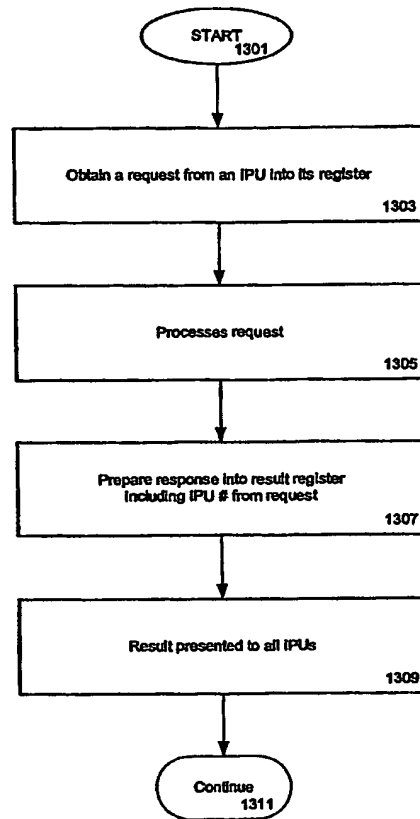


FIG. 13

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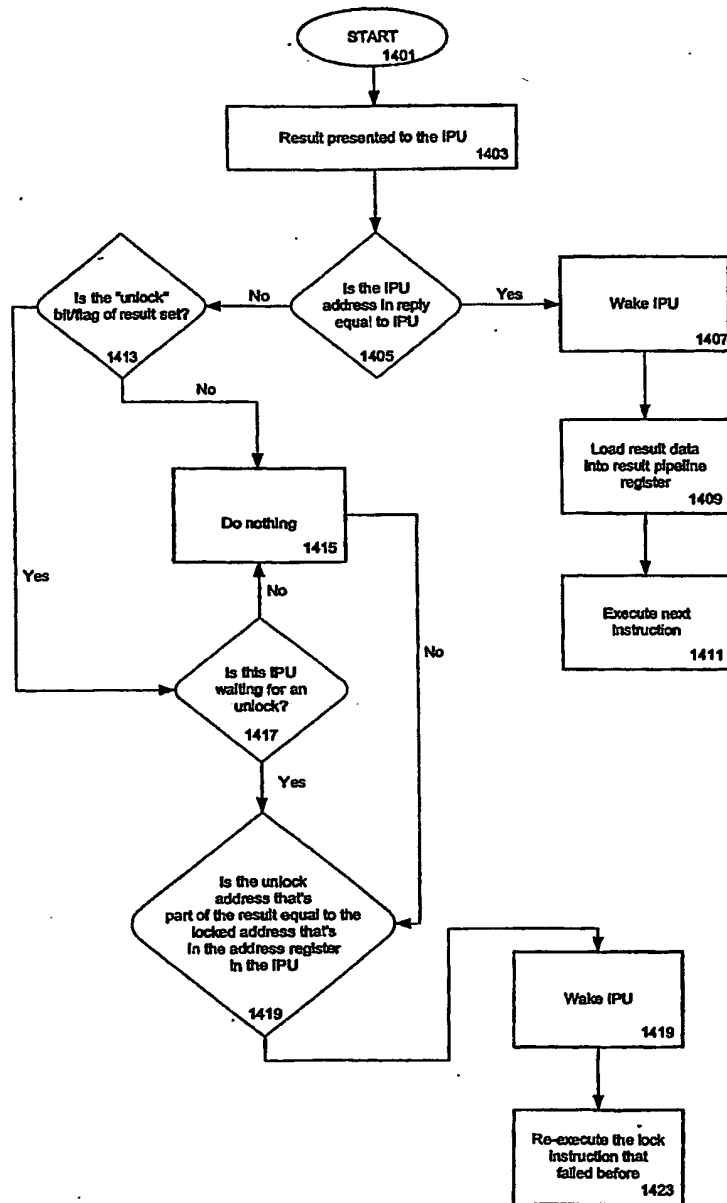


FIG. 14

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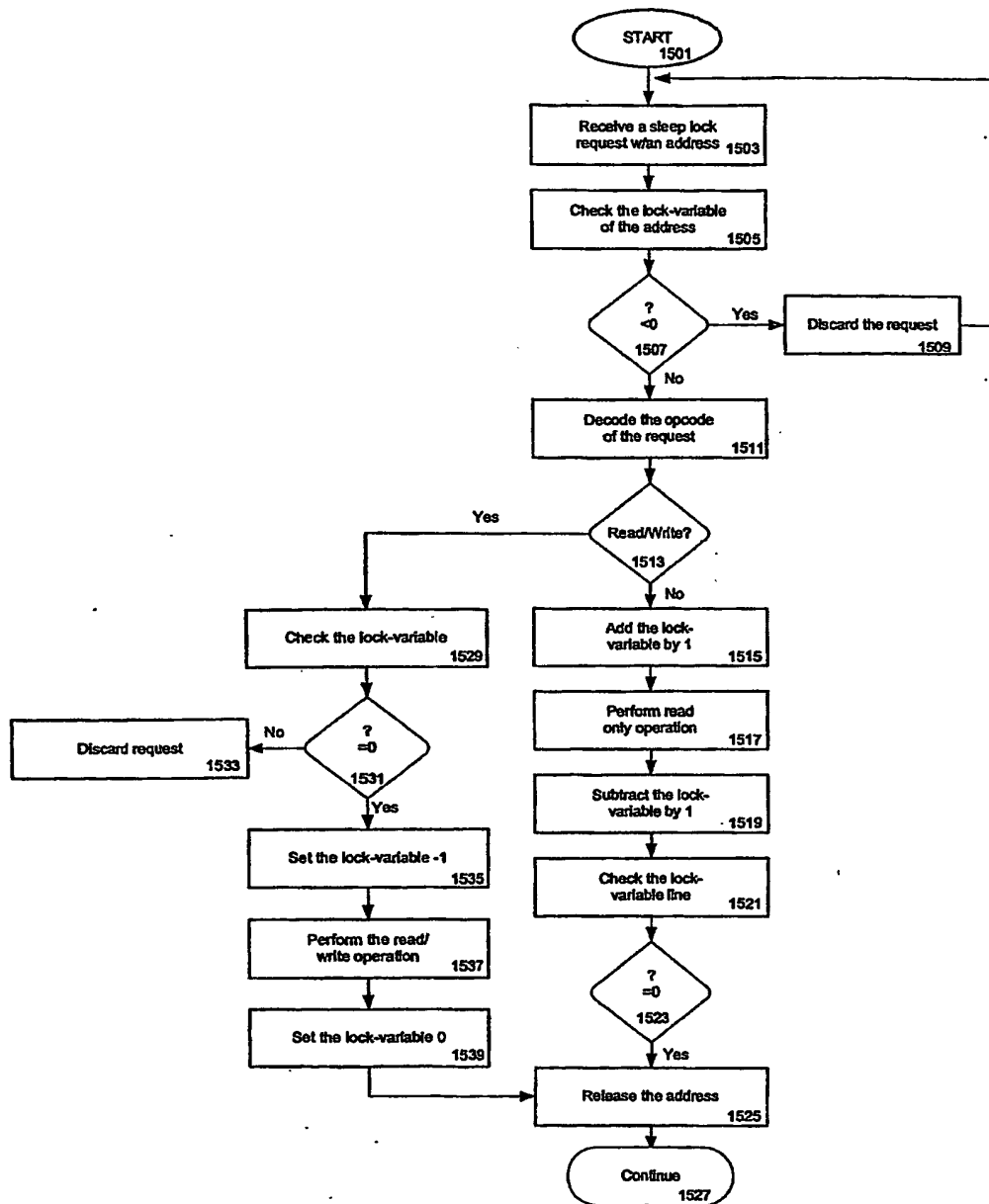


FIG. 15

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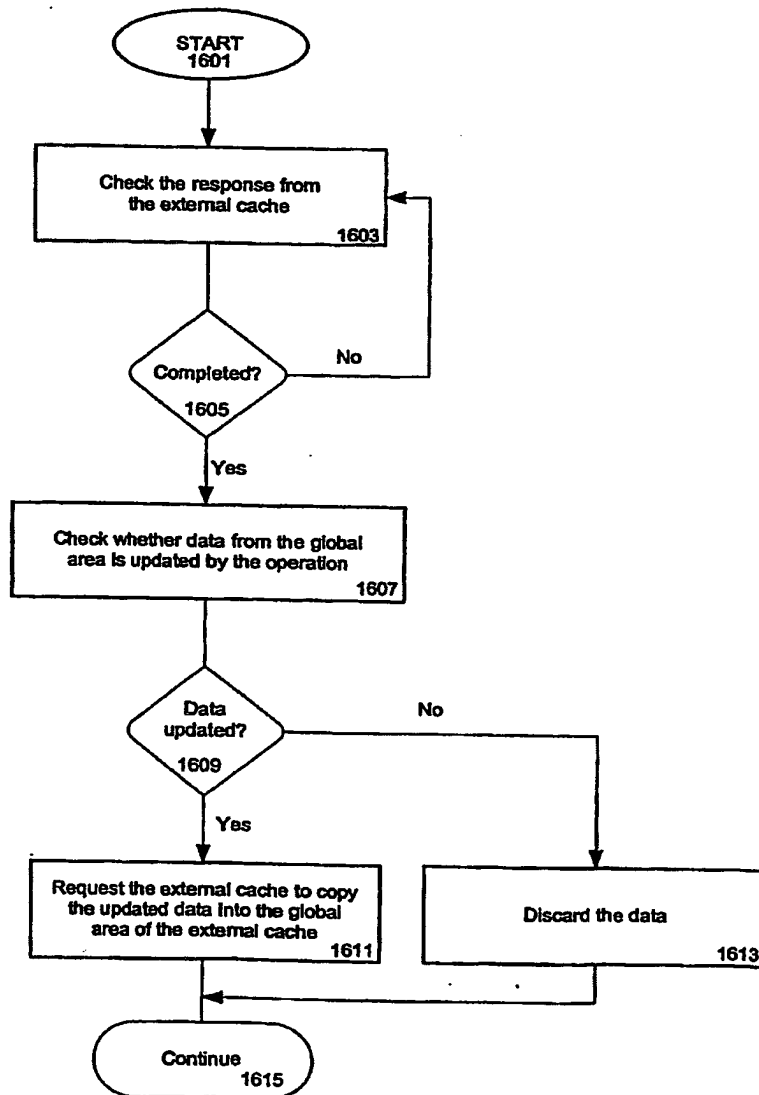


FIG. 16



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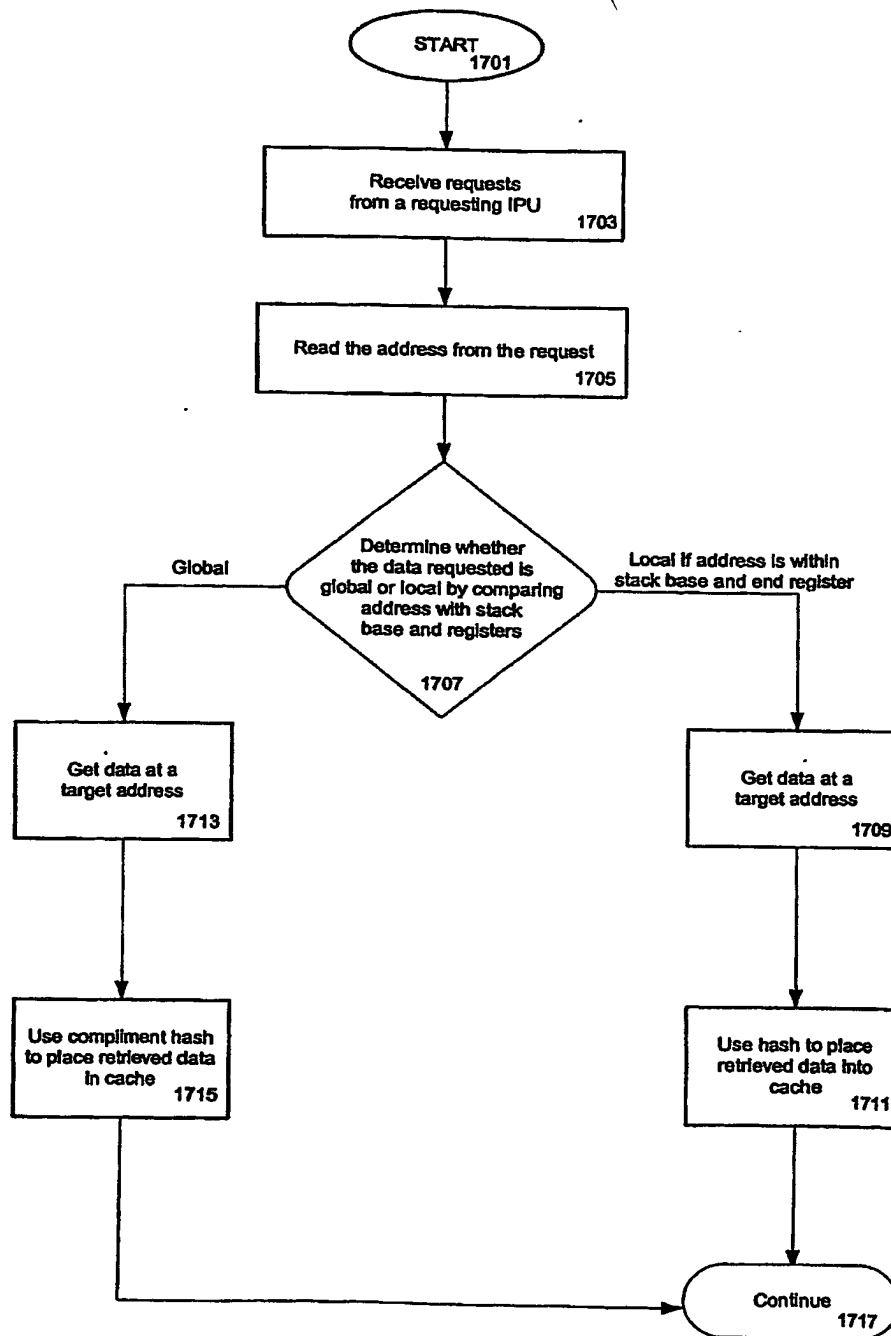


FIG. 17

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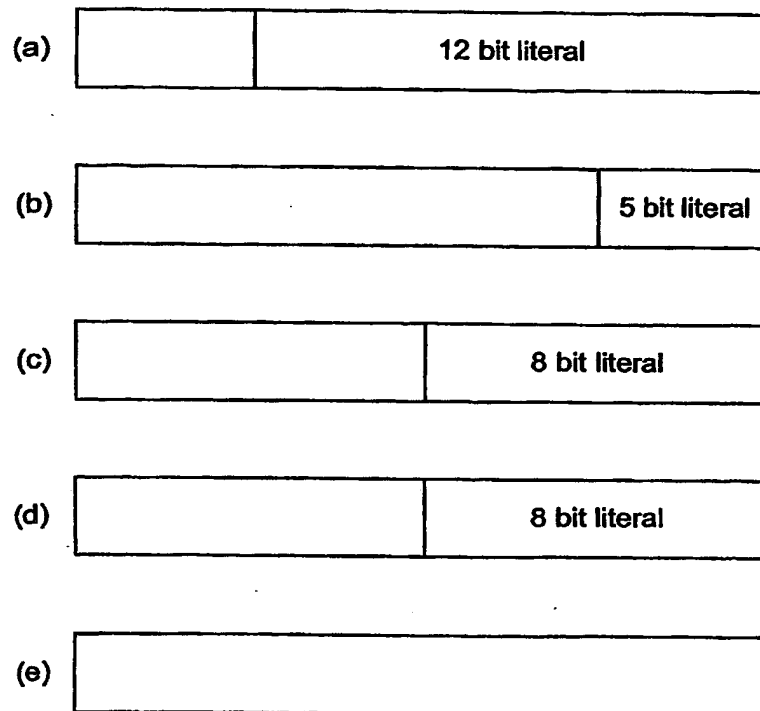


FIG. 18

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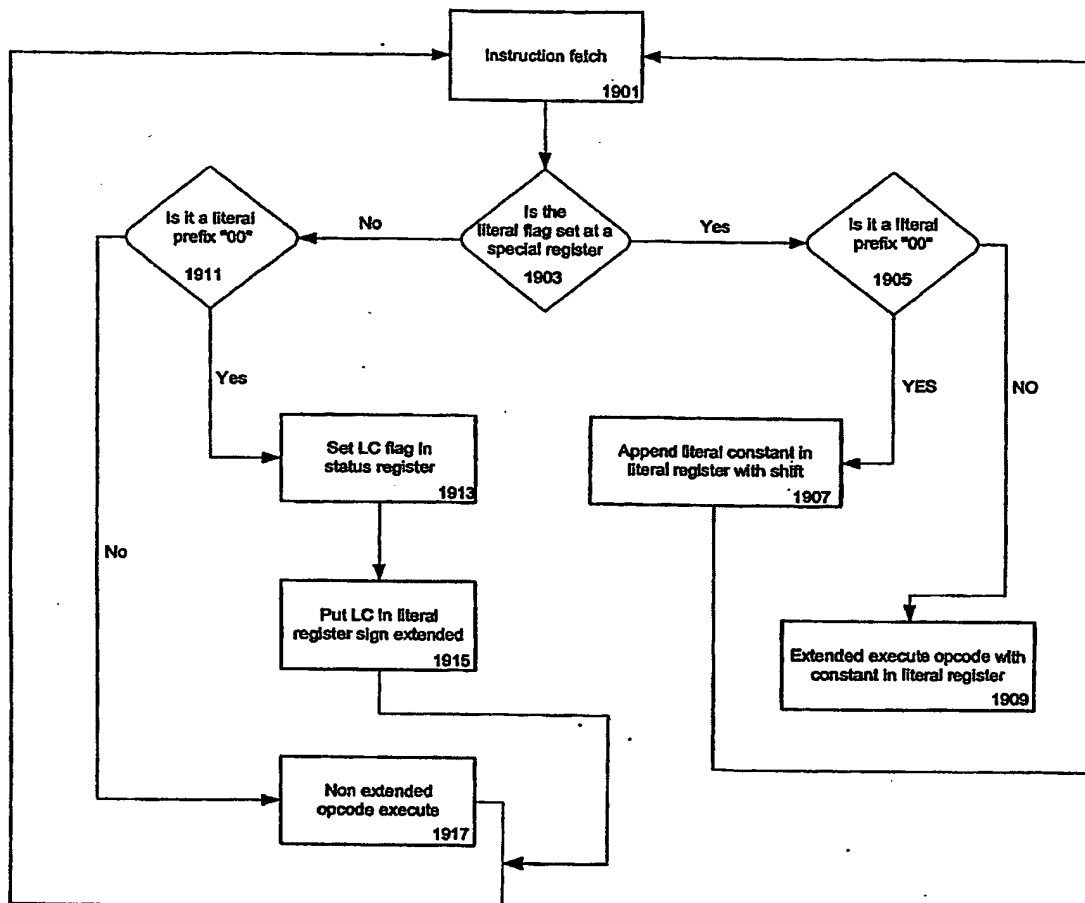


FIG. 19

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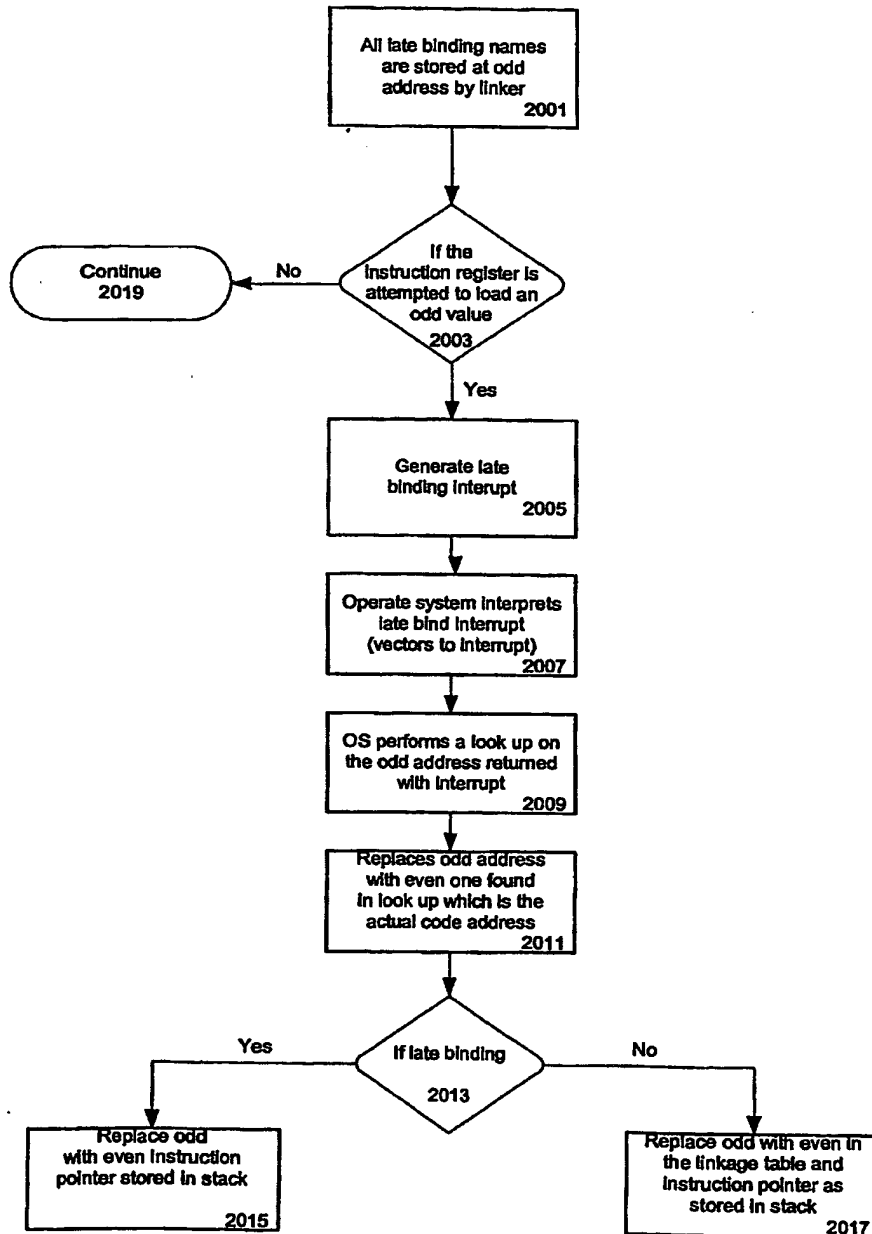


FIG. 20

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## Status Register

Cycle Flags	Operations requesting number of cycles
0 (2101)	Normal (simple cycle) (2109)
1 (2103)	Double (two cycles/double processes load/save) (2111)
2 (2105)	Extend (multi cycles/double processes load/save) (2113)
3 (2107)	Repeated (multiple cycles/single/double process status) (2115)

FIG. 21

Type Flag	Number of Registers	Number of Bits	Type
0 (2201)	8 (2205)	32 (2209)	Data (2213)
1 (2203)	8 (2207)	32 (2211)	Address (2215)

FIG. 22

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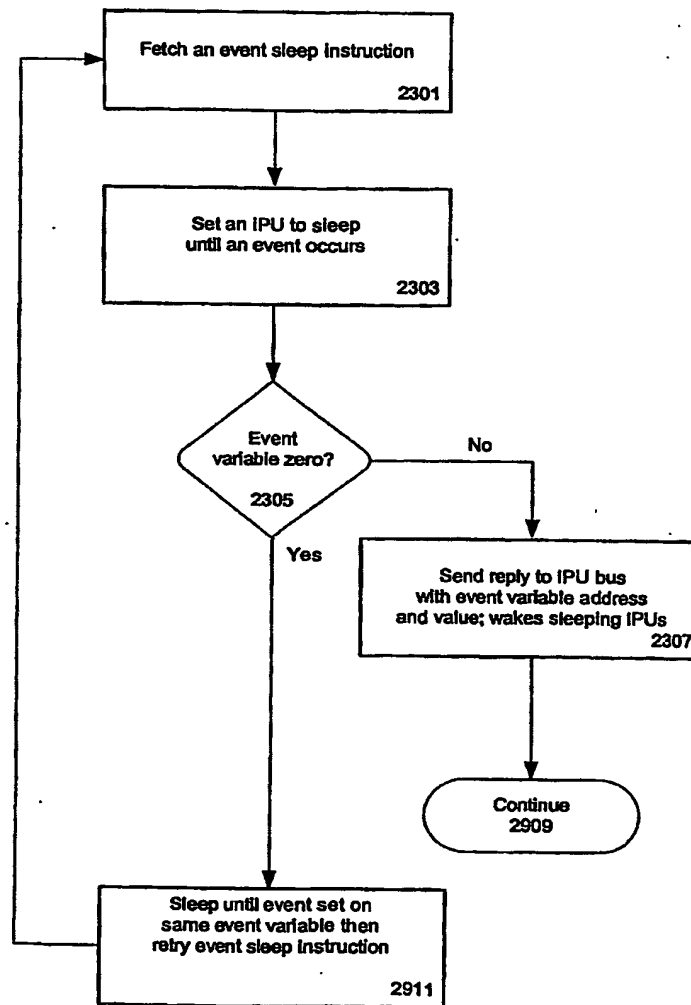


FIG. 23

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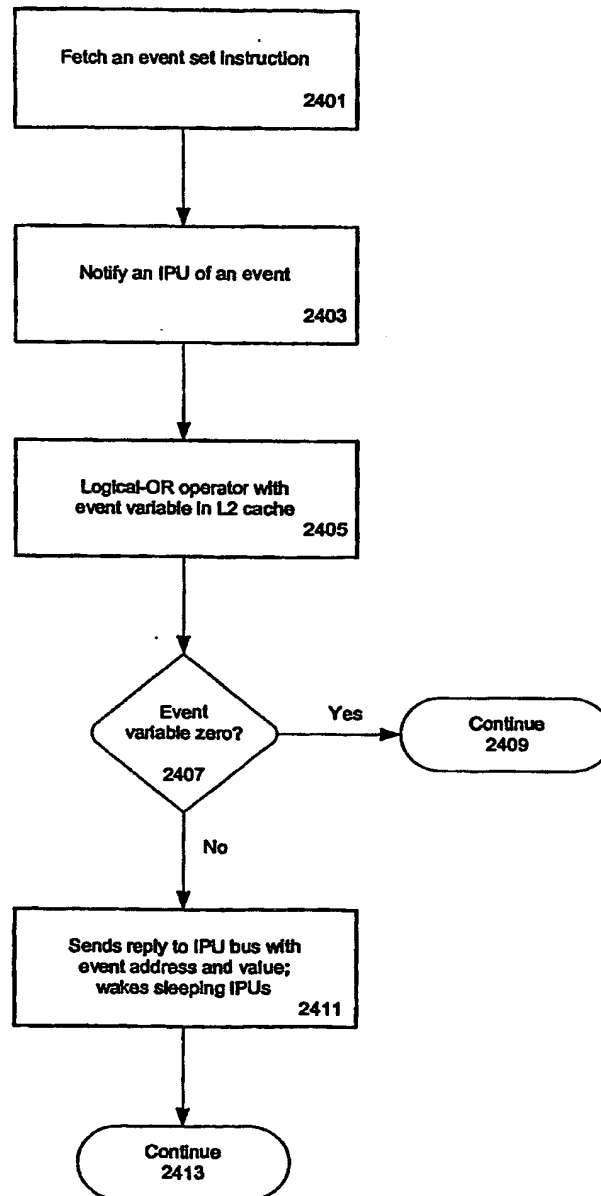


FIG. 24

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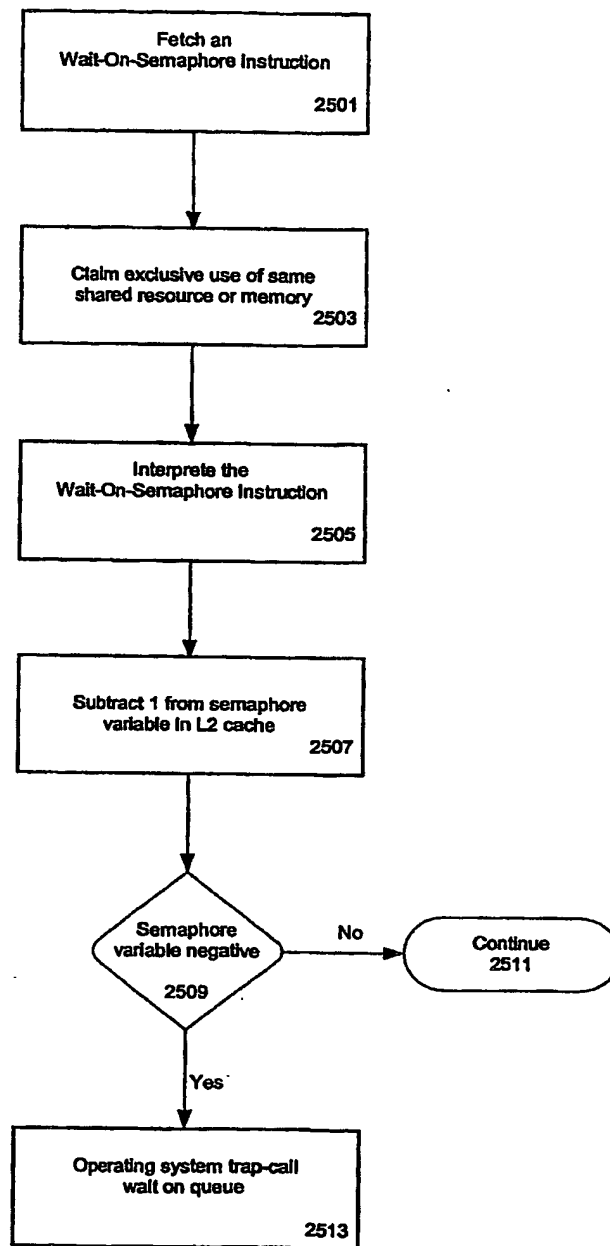


FIG. 25



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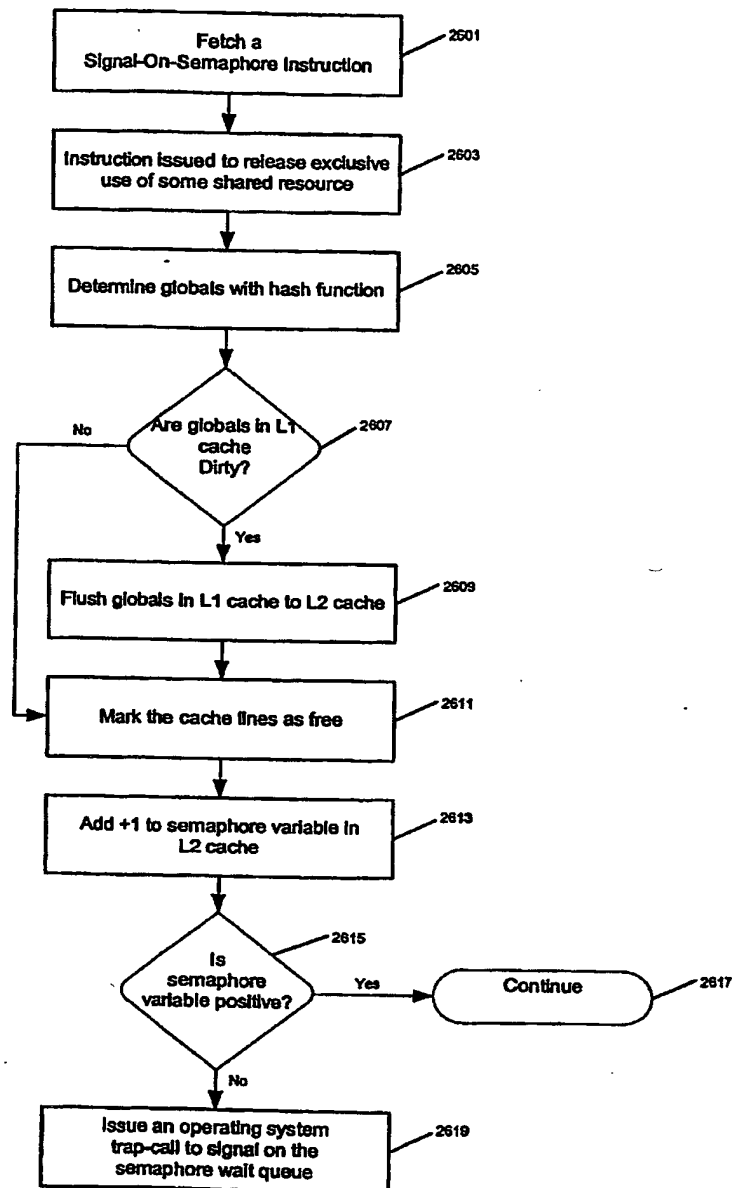


FIG. 26

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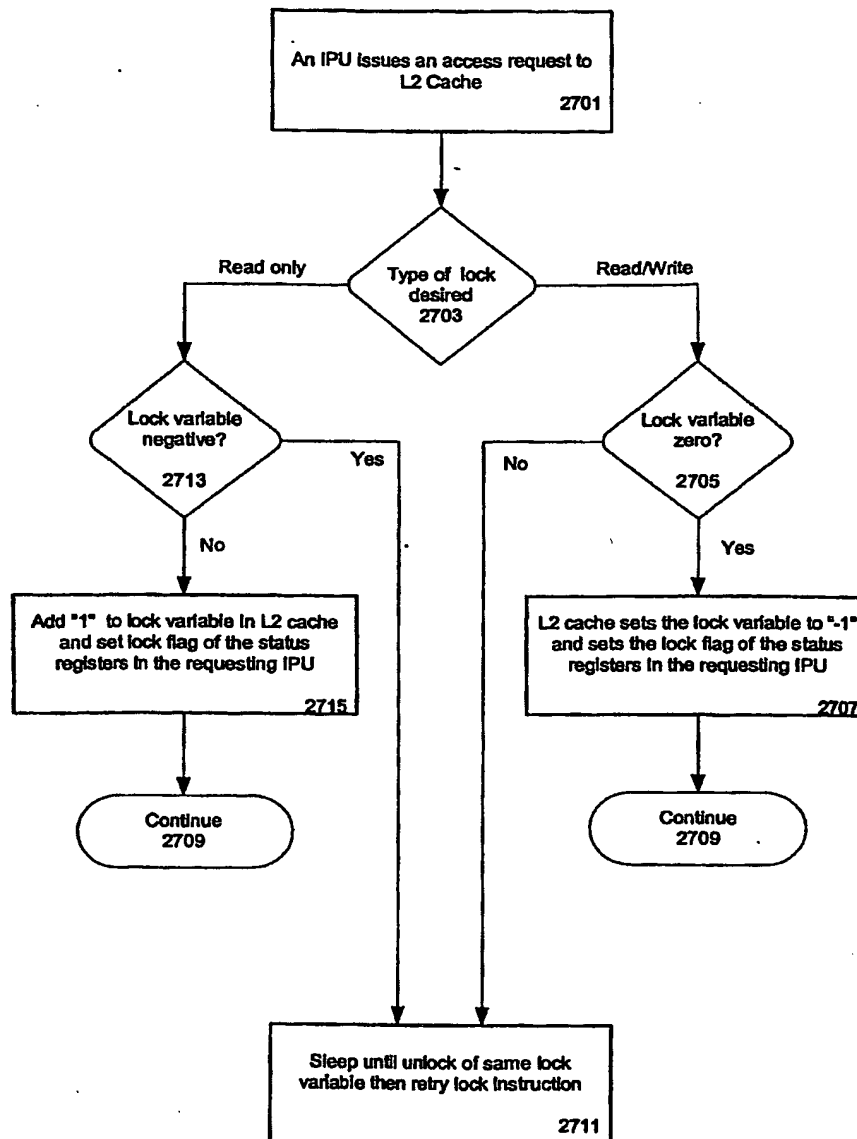


FIG. 27

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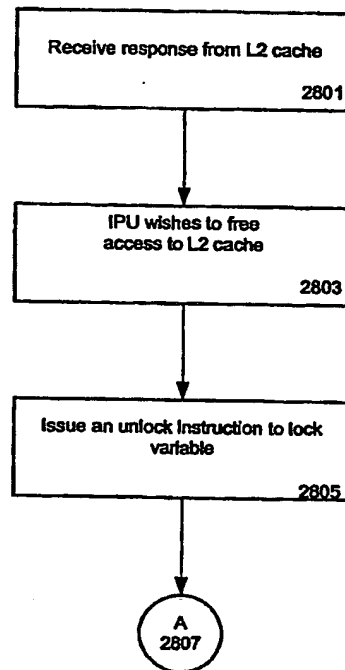


FIG. 28

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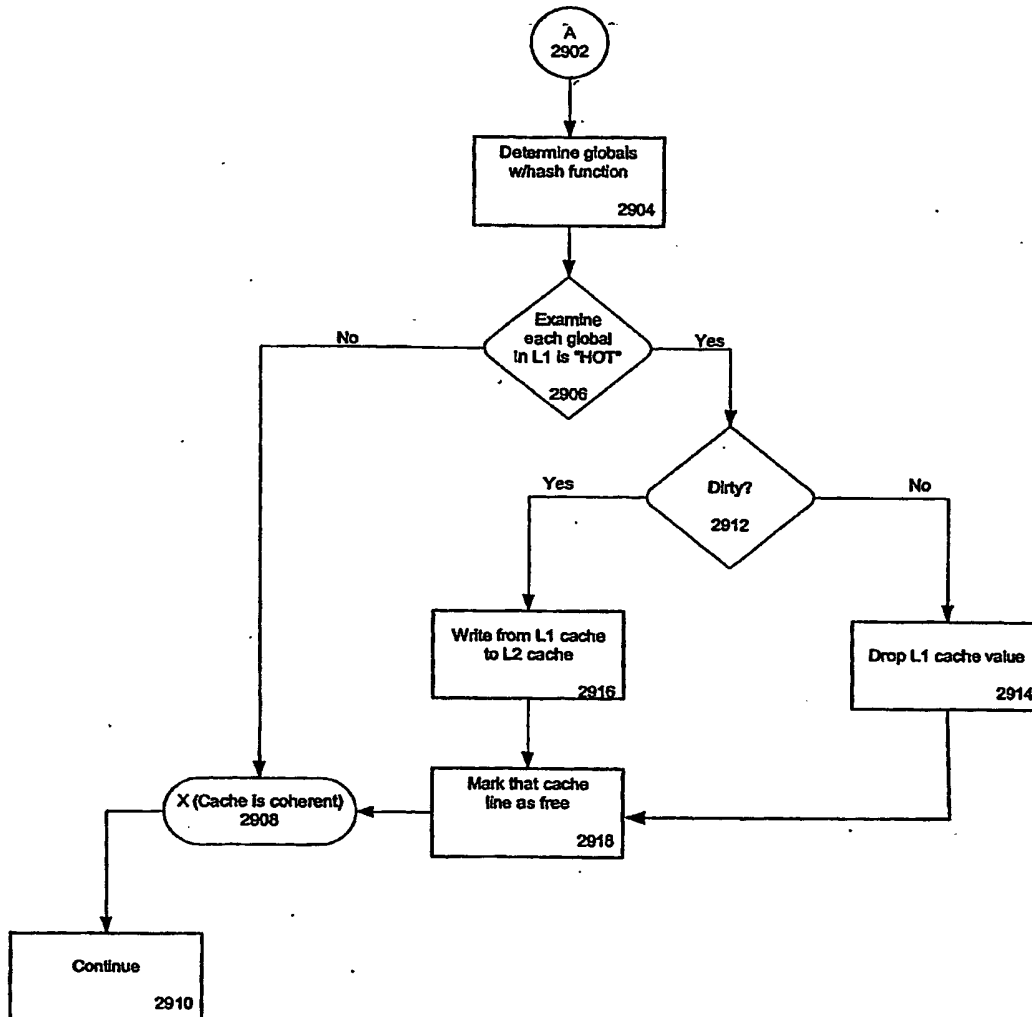


FIG. 29

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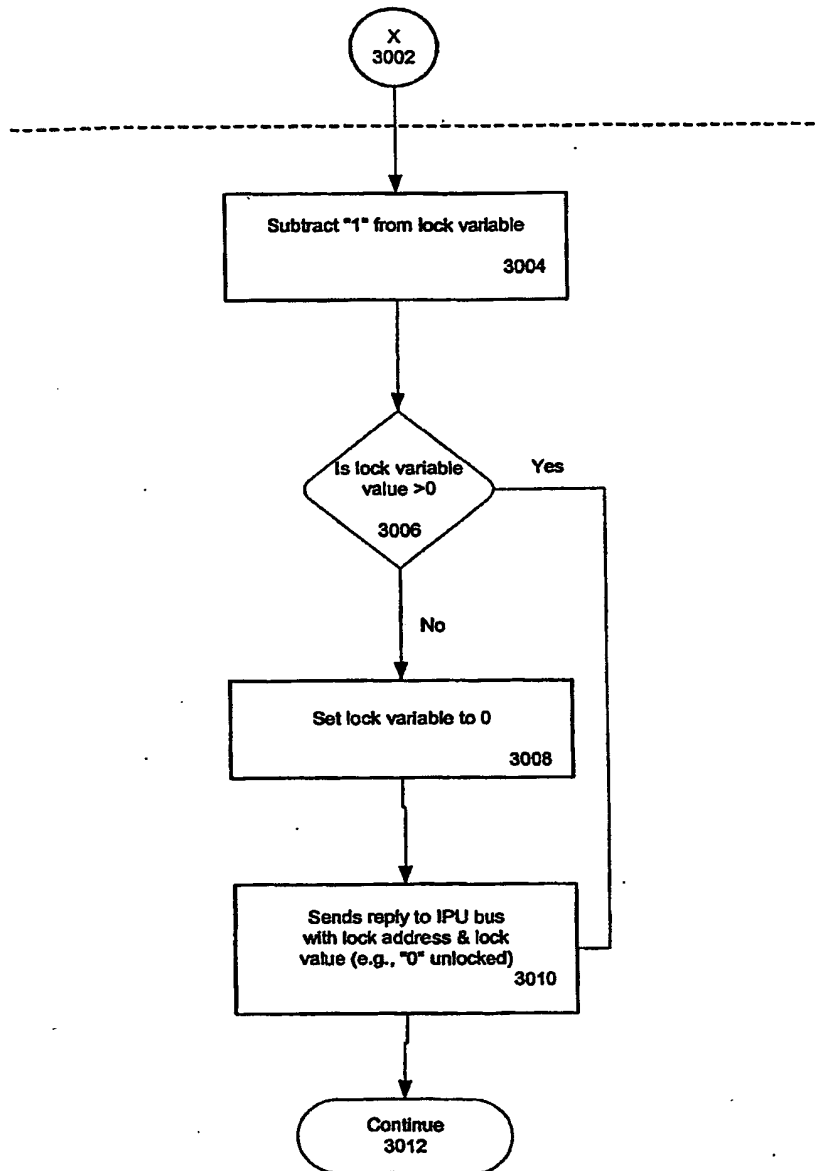


FIG. 30

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